WHAT IS CLAIMED IS:

1. A timing adjustment circuit, comprising:

an input circuit for outputting an external clock signal supplied from the outside as an input clock signal;

a delay adjustment circuit for delaying the input clock signal from the input circuit to output a delayed input clock signal; and

a clock driver for outputting an internal clock signal in response to the delayed input clock signal from the delay adjustment circuit, so as to determine delay of the delay adjustment circuit so that a phase of an output signal outputted from a circuit to be driven in synchronization with the internal clock signal has a predetermined relation with respect to that of the external clock signal, when the internal clock signal is used to drive the circuit to be driven,

the timing adjustment circuit further comprising a phase advance/delay signal generation unit for using the internal clock signal and either one of the external clock signal and the output signal of the circuit to be driven to produce a phase advance/delay signal indicating whether the phase of the output signal from the circuit to be driven advances or delays with respect to the phase of the external clock signal.

2. The timing adjustment circuit according to claim 1, further comprising:

a replica circuit for delaying a branched clock signal obtained by branching the internal clock signal in order to feedback-control the delay of the delay adjustment circuit; and

a phase comparison circuit for comparing the phase of the output signal of the replica circuit with that of the external clock signal and outputting a comparison result to the delay adjustment circuit to adjust the delay of the delay adjustment circuit,

the timing adjustment circuit further comprising:

a replica circuit which is used as the replica circuit and which is capable of adjusting the delay;

a selection circuit for selectively outputting either one of the external clock signal and the output signal from the circuit to be driven to the phase comparison circuit; and

an external output unit for outputting an output of the phase comparison circuit to the outside,

wherein the selection circuit selects the output signal from the circuit to be driven to operate a combination of the selection circuit, the replica circuit, and the phase comparison circuit as the phase advance/delay signal generation unit, and the comparison result of the phase comparison circuit is supplied as the phase advance/delay signal to the external output unit.

3. The timing adjustment circuit according to claim 2, wherein:

the replica circuit is constituted to be capable of adjusting a delay time by change of a content held in a register or by disconnection of a fuse.

4. A semiconductor device, comprising:

the timing adjustment circuit according to claim 1; and

a data output circuit for functioning as a circuit to be driven by an internal clock signal supplied from the timing adjustment circuit to output data at a timing defined by the internal clock signal.

5. A semiconductor device, comprising:

the timing adjustment circuit according to claim 3 capable of adjusting both a delay time by change of a content held by a register and a delay time by disconnection of a fuse; and

a data output circuit for outputting data at a timing defined by the internal clock signal, which is a circuit to be driven by an internal clock signal supplied from the timing adjustment circuit,

wherein a tester connected to the external output unit is used to monitor the phase advance/delay signal while the content held by the register is changed to obtain an appropriate delay time, and subsequently the fuse is disconnected so that the delay time of the timing adjustment circuit can be fixed to the appropriate delay time.

6. The timing adjustment circuit according to claim 1, wherein:

the delay adjustment circuit is constituted to be capable of changing the delay time,

the circuit to be driven is a data input circuit for latching input data supplied from the outside in synchronization with the internal clock signal, and

the phase advance/delay signal generation unit includes the same constitution as that of the circuit to be driven and comprises a unit for receiving supply of the external clock signal instead of the input data to latch the external clock signal in synchronization with the internal clock signal and for outputting the phase advance/delay signal to the outside.

7. The timing adjustment circuit according to claim 6, wherein:

the delay adjustment circuit is constituted to be capable of adjusting the delay time by change of a content held by a register or by disconnection of a fuse.

8. A semiconductor device, comprising:

the timing adjustment circuit according to claim 6 ; and

a data input circuit for latching input data supplied from the outside at a timing defined by the internal clock signal, which is a circuit to be driven by an internal clock signal supplied from the timing adjustment circuit.

9. A semiconductor device, comprising:

the timing adjustment circuit according to claim 7 capable of adjusting both a delay time by change of a content held by a register and a

delay time by disconnection of a fuse; and

a data input circuit for latching input data supplied from the outside at a timing defined by the internal clock signal, which is a circuit to be driven by an internal clock signal supplied from the timing adjustment circuit,

wherein a tester connected to the phase advance/delay signal generation unit is used to monitor the phase advance/delay signal while the content held by the register is changed to obtain an appropriate delay time, and subsequently the fuse is disconnected so that the delay time of the timing adjustment circuit can be fixed to the appropriate delay time.